Three-dimensional integration of metal-oxide-semiconductor transistor with subterranean photonics in silicon

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Monolithic integration of photonics and electronics has been achieved in silicon by three-dimensionally integrating metal-oxide-semiconductor field-effect transistors and waveguide-coupled microdisk resonators. Implantation of oxygen ions into a silicon-on-insulator substrate with a patterned thermal oxide mask followed by a high temperature anneal was utilized to realize the buried photonic structures. This results in the formation of vertically stacked silicon layers separated from each other by an intervening oxide layer. Transistors are fabricated on the surface silicon by conventional processing techniques. Optical and electronic functionalities are thus separated into two different layers of silicon, paving the way toward dense three-dimensional optoelectronic integration. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2184754]

Silicon-on-insulator (SOI) materials system has proven to be an efficient platform for the realization of both electronic and photonic devices. Recent years have seen significant amounts of research in the area of silicon photonics, resulting in the demonstration of a variety of both active and passive optical functionalities.[1–8] These technologies have demonstrated the feasibility of using silicon for the realization of integrated optical devices. One of the most attractive features of the silicon is the prospect of full integration of optical and electronic devices on the same substrate. However, the trend of down scaling transistor dimensions in silicon ultralarge scale integration (ULSI), with the number of transistors per chip projected to reach around 1 billion (10^9), has heightened the economic incentive to utilize silicon real estate most efficiently. It is therefore necessary to develop innovative fabrication technologies that would make the integration of optical and electronic devices viable on silicon substrates, without compromising the real-estate economics of wafer manufacturing. In order to utilize the foundry capabilities in silicon, it is necessary that these technologies be compatible with the well established complementary metal-oxide-semiconductor (CMOS) processing techniques.

We have previously reported the technique of separation by implantation of oxygen (SIMOX) three-dimensional (3D) sculpting that was used to realize optical devices on vertically stacked layers of silicon separated by a silicon dioxide layer. A variety of optical devices such as low loss optical waveguides, vertically coupled microdisk resonators[9] and add-drop filters[10] have been realized using this technique. In addition, this approach was also extended to obtain subterranean waveguide-coupled resonators, thus confining the optical circuitry to a buried silicon layer.[11] This leaves a surface silicon layer, separated from the buried silicon layer by an intervening silicon dioxide layer, for the realization of electronic devices. In this letter, we demonstrate monolithic optoelectronic integration in silicon by realizing metal-oxide-semiconductor field-effect transistors (MOSFETs) on the surface layer silicon of a double-layer silicon-on-insulator (SOI) wafer that has laterally coupled microdisk resonators in a buried silicon layer. More significantly, optoelectronic integration is achieved by confining the optical circuitry to a subterranean silicon layer. Thereby, silicon real estate on the surface is not consumed, allowing it to be used for the realization of electronic circuitry. Thus, the technology reported in this letter is different from the planar approach to optoelectronic integration where optical and electronic devices are fabricated on the same silicon layer. Planar integration has been utilized to obtain photodetectors and other optical devices integrated with silicon-based MOSFETs in a monolithic fashion.[12] It may be noted, however, that this approach to integration impacts the availability of silicon real estate.

The process of SIMOX 3D sculpting has been discussed in detail elsewhere.[10] Briefly, the process begins with the implantation of oxygen ions into an SOI substrate patterned with thermally grown oxide. The thickness of the thermal oxide mask may be chosen suitably to decelerate the oxygen ions that penetrate into the area underneath the mask during the implantation. After the implantation, annealing is performed at high temperatures (~1300 °C) to cure the implantation damage and to aid in the formation of a continuous buried SiO_2. This buried SiO_2 layer separates the surface silicon of the SOI wafer into a buried silicon layer below it and a surface silicon layer above it. These layers will henceforth be referred to as the buried silicon layer and the surface silicon layer. Thus, by employing the process of masked implantation followed by annealing, rib waveguide-based devices can be realized in the buried silicon layer. On the surface silicon layer, conventional processing can be used to define a variety of electronic and photonic devices.

Figure 1 shows the cross-sectional scanning electron micrograph (SEM) of a rib waveguide in the buried silicon layer that is fabricated using the technique of SIMOX 3D sculpting. These waveguides act as bus waveguides to the microdisk resonators that are realized in the same buried silicon layer. It can be seen that the method of masked oxygen implantation and subsequent annealing has resulted in the formation of a 220 nm buried rib silicon layer which is separated from a 240 nm thick surface silicon layer by a continuous layer of SiO_2 of uniform thickness of ~100 nm. In this

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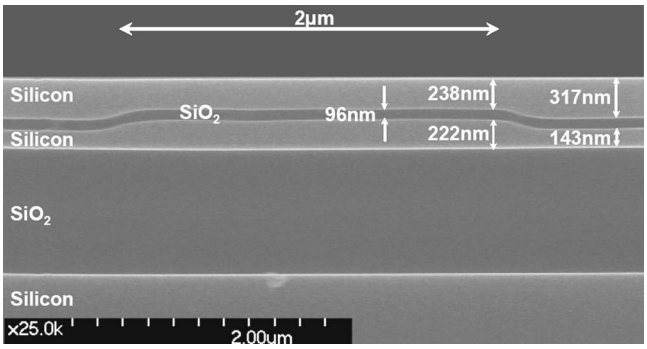

FIG. 1. Cross-sectional SEM of rib waveguides realized in the buried silicon layer. These waveguides act as bus waveguides to the microdisk resonator.

case, the SOI substrate was implanted at 150 keV, with an oxygen ion dose of $5\times10^{17}/\mathrm{cm}^2$.

After the fabrication of optical devices in the buried silicon layer, conventional processing is used to the realize MOSFETs on the surface silicon layer. The wafers are subjected to a uniform boron implantation and subsequent anneal activation and drive-in to achieve a doping of $2\times10^{17}\ \mathrm{cm}^{-3}$ in the body region. Then, the active area where transistors are to be fabricated is defined via lithography, and field oxidation is performed everywhere except in the active region to obtain electrical isolation of the devices on the surface silicon layer. Subsequently, gate oxidation and polysilicon deposition are performed, followed by lithography to define the gate region. A gate oxide of thickness 25 nm is used in this work. A self-aligned phosphorus implant is then employed to define the source and drain regions of the transistor. Photolithography followed by a subsequent boron implantation step is used to obtain the body contact. The dopants are then activated using rapid thermal annealing (RTA) in nitrogen ambient. A layer of low temperature oxide (LTO), of thickness 500 nm, is deposited and patterned to define vias for electrical contact during the deposition of metal. Aluminum sputtering, followed by lithography and wet etching, is then used to define the metal pads required for the electrical probing of these devices. Figure 2 shows an optical micrograph of an MOS transistor fabricated on the surface silicon layer, on top of a microdisk resonator that is situated in the buried silicon layer. These resonators consist

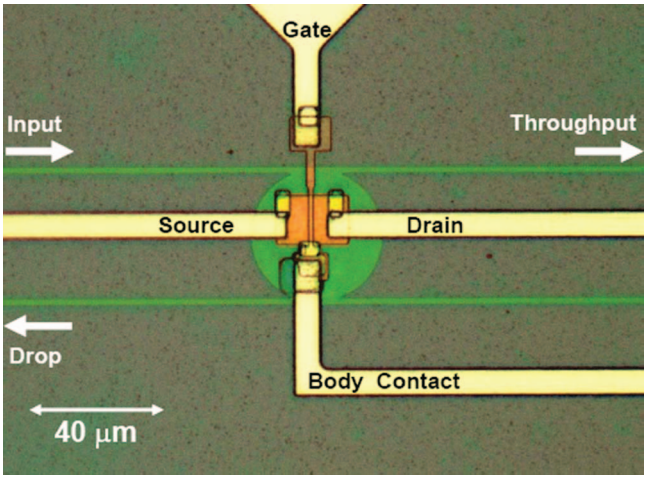

FIG. 2. (Color) Optical micrograph of a MOS transistor fabricated on the surface silicon layer, on top of a microdisk resonator that is situated in the buried silicon layer.

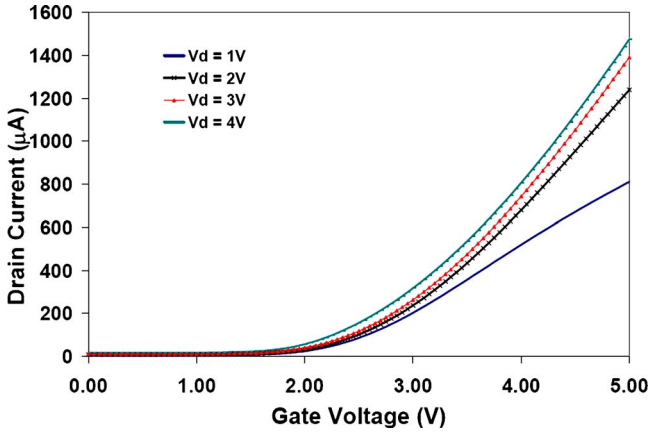

FIG. 3. Gate control characteristics (I_D vs V_G) of the fabricated MOSFET.

of 2 μm wide waveguides acting as input and output ports to a microdisk with a radius 20 μm. One of the bus waveguides acts as the input port where the optical power is launched. The resonant wavelengths are directed to the drop port of the device, whereas those wavelengths that are out of resonance are collected at the throughput port of the device, as denoted in Fig. 2.

The optical characterization of the microresonator filters in the buried silicon layer has been discussed in detail in our previous work.[11] In summary, we observe the spectrum at the throughput port of the resonator using an optical spectrum analyzer. A broadband optical source is used as the input to the device for this purpose. The throughput port spectrum shows sharp resonances with a free spectral range of 5 nm and optical extinction ratios as high as 20 dB. In a microdisk resonator based on whispering gallery modes, most of the optical energy is confined to the periphery of the disk structure. As evident from Fig. 2, MOSFETs are contained entirely within the disk, away from the peripheries of the microdisk. Further, the surface silicon layer directly above the peripheries of the microdisk is thermally oxidized during the active area isolation step of the fabrication process, as described earlier in the text. Thus, the realization of MOSFETs on the surface silicon layer is not expected to affect the performance characteristics of the resonators in the buried silicon layer in any significant manner.

The electrical characteristics of these *n*-channel MOSFETs were extracted using a HP4145B semiconductor parameter analyzer. Figure 3 shows the drain current (I_D) versus gate voltage (V_G) characteristics demonstrating gate control in the fabricated MOSFETs. Figure 4 shows the drain current versus drain voltage (V_D) characteristics of the inversion channel. These transistors had a gate length of 1 μm. The devices exhibit a threshold voltage of 2.5 V, which is close to the theoretically expected value. These characteristics clearly illustrate the realization of MOS transistors that are monolithically integrated with buried optical devices. As a simple application of this technology, switches based on the thermo-optic effect may be fabricated to tune the resonator, where switching is achieved by the MOSFET controlling the current to the heater element.

It can be noticed that in the subthreshold region, nonzero leakage currents are observed. It has been previously observed that, in the presence of defects in the silicon wafer, there can be diffusion of dopants from source and drain regions.[13] This can result in electrically active leakage paths

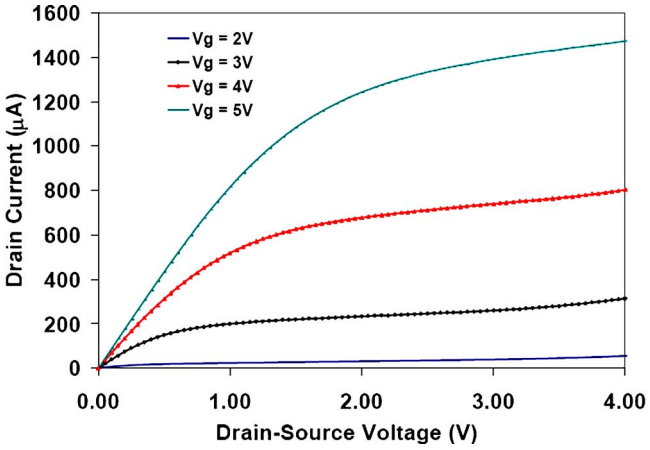

FIG. 4. Drain characteristics (I_D vs V_D) of the fabricated MOSFET.

from source to the drain, contributing to leakage currents in subthreshold regime. It is known that the SIMOX process can result in the creation of defects during the implantation of oxygen ions.[14] After the annealing of the wafers subsequent to oxygen implantation, we measured defect densities of the order of 5×10^4 cm^{-2} using Secco etching. We believe that these defects are responsible for the leakage currents observed. Currently, process optimization is in progress to further lower the defect densities.

It must be emphasized that we have demonstrated a technique that results in the integration of both optical and electronic devices on the same substrate monolithically. More significantly, this integration does not impact the availability of silicon real estate from the point of view of ULSI electronic circuitry as the optical and electronic functionalities are separated to two different layers of silicon. This presents an innovative approach toward monolithic optoelectronic integration in silicon that is compatible with the conventional CMOS foundry processing techniques.

In conclusion, SIMOX 3D sculpting has been used to monolithically integrate MOS transistors and photonic devices in vertically stacked silicon layers. These layers are separated from each other by an insulating dielectric that provides electrical isolation to electronic devices above it and optical confinement to photonic devices below it. The proposed technology presents an efficient approach to integrate electronic and optical devices on SOI substrates in a way that is compatible with CMOS foundry processing methods.

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