to implement the total impedance. Typically the shunt circuit requires large inductor values (up to 1000s of Henries), therefore Riordan gyrators [3] are required to implement the inductor elements. Gyrator circuits are large in size and are sensitive to component tolerances. Also, PZTs are capable of generating large voltages for moderate structural excitations, therefore the gyrators must be constructed from high-voltage operational amplifiers. Furthermore, the required number of operational amplifiers required to shunt-dampen two structural modes could be > 32 op-amps.

In this Letter we introduce a method for implementing an impedance of arbitrary order and complexity. This 'synthetic impedance' is used in place of shunt-damping networks to provide effective vibrational damping without the problems associated with direct circuit implementations.

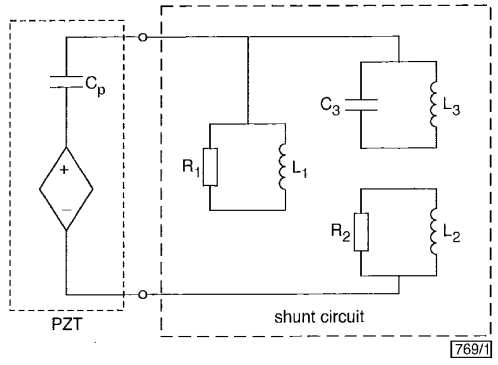

Fig. 1 *Simplified shunt-damping circuit of [2]*

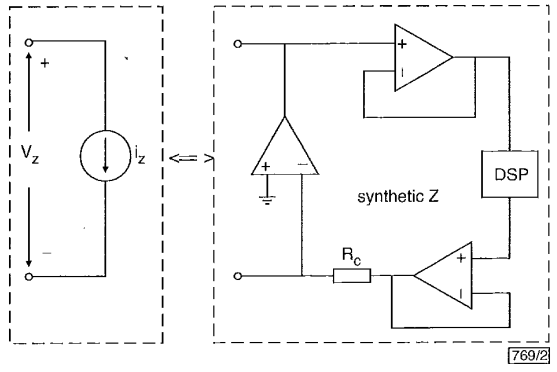

Fig. 2 *Synthetic impedance*

Synthetic impedance: We define a synthetic impedance as a two-terminal device that establishes some arbitrary relationship between voltage v_z and current i_z at its terminals. The functionality of the device is shown in Fig. 2, where: $i_z(t) = f(v_z(t))$. This can be made to synthesise any network of physical components by fixing i_z as the output of a linear transfer function of v_z, $I_z(s) = Y(s)V_z(s)$, where $Y(s) \equiv 1/Z(s)$ and $Z(s)$ is the desired impedance to be seen from the terminals. A DSP system *dSPACE* is used to simulate the required transfer function $Y(s)$ in real time, as shown in Fig. 2.

Application: To validate the shunting simulated impedance, experiments were carried out on a simply supported piezoelectric laminated beam, i.e. a mechanically resonant structure. The resonant beam structure consists of a uniform aluminum beam of rectangular cross-section with experimentally pinned boundary conditions at both ends. A pair of piezoelectric ceramic patches (PIC151) are attached symmetrically to either side of the beam surface. One of the patches is used as an actuator and the other as a shunting layer, i.e. sensing layer.

The synthetic impedance can now be used in place of the passive network shown in Fig. 1. The desired impedance is first calculated, then the corresponding admittance transfer function is implemented on the *dSPACE* DSP system.

The simply supported beam is excited by applying a voltage signal V_a to the piezoelectric actuator. To determine the damping performance of the synthetic impedance, the frequency response of the beam from the structural excitation voltage to the structural displacement at a point on the beam surface can be measured, i.e. $d(x, s)/V_a(s)$. The frequency response is captured using a polytec scanning vibrometer (PSV-300). The uncontrolled and damped frequency response $d(x, s)/V_a(s)$ of the beam is plotted in Fig. 3. Results show that the synthetic impedance dampens two structural modes of the piezoelectric laminated beam by 18 and 20dB.

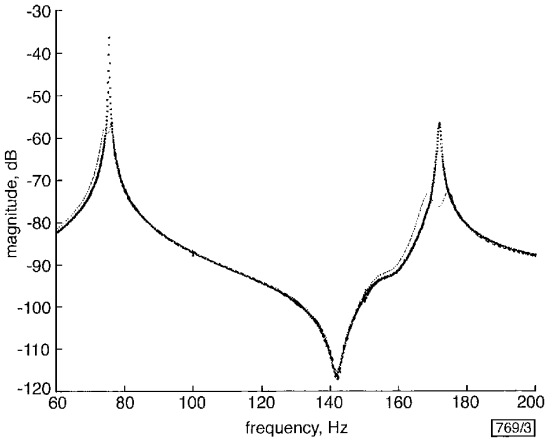

Fig. 3 *Frequency response of piezoelectric laminated simply supported beam*

..... experimental (undamped)
——— experimental (damped)

Conclusions: A method has been presented for implementing a simulated impedance required for effective shunt-damping of a resonant structure. This technique has alleviated some of the practical problems associated with shunt-damping. The arbitrary impedance has also created the opportunity for more advanced passive control solutions. This includes passive controllers that adapt to structural variations, i.e. adaptive controllers.

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30Gsample/s time-stretch analogue-to-digital converter

A.S. Bhushan, P. Kelkar and B. Jalali

High speed analogue-to-digital conversion using a photonic time-stretch preprocessor followed by an electronic digitiser is demonstrated. The preprocessing increases the effective sampling rate and input bandwidth of the digitiser. The system exhibits 30Gsample/s sampling rate with 26dB signal-to-noise ratio over a 4GHz bandwidth.

It is widely recognised that the analogue-to-digital converter (ADC) is the bottleneck in most high performance radar and communication systems. The performance of the ADC has not kept pace with rapid improvements in the digital signal processor (DSP), preventing exploitation of the latter's true capability. Hence new concepts that could offer revolutionary improvements in ADC performance are of paramount importance.

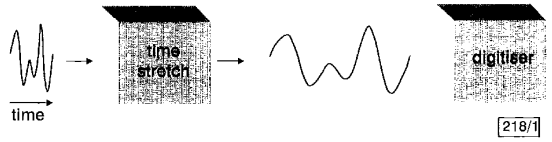

Fig. 1 *Block diagram for time-stretch analogue to digital converter*

Recently we have proposed the concept of a time-stretch ADC (TSADC) [1, 2]. The system shown in Fig. 1 consists of an optoelectronic time-stretch preprocessor (TSP) followed by an electronic digitiser. The TSP reduces the bandwidth of the electrical signal by a factor of M, effectively increasing both the sampling rate and the input bandwidth of the digitiser by M. The technique is well suited for time-limited analogue signals, such as those encountered in pulsed radar. It can also be extended to continuous-time input signals [1, 2].

In this Letter, we demonstrate the viability of time-stretch preprocessing (TSP) as a means to dramatically enhance the capabilities of an electronic digitiser. A complete TSADC system with 30Gsample/s sampling rate and 26dB signal-to-noise ratio (SNR) measured over a 4GHz bandwidth is demonstrated. The system consists of a photonic TSP and an electronic digitiser with 8Gsample/s, 1.5GHz bandwidth and 32dB SNR.

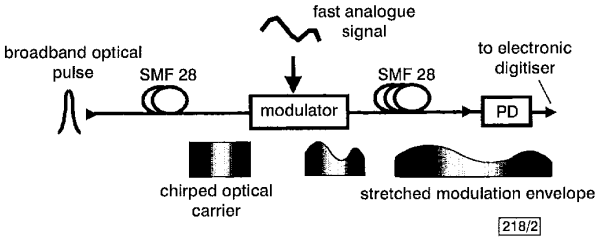

Fig. 2 *Photonic time-stretch preprocessor*

A block diagram of the TSP is shown in Fig. 1 and the experimental setup is shown in Fig. 2. A broadband near-transform-limited optical pulse, generated by a passively modelocked fibre laser, is dispersed by transmission in 2km of singlemode fibre (SMF28). The dispersion separates the spectral components of the optical pulse in time, creating time to wavelength mapping. The electrical signal (5GHz sine wave) modulates the chirped optical carrier in an $LiNbO_3$ Mach-Zehnder modulator. Hence each time instant on the electrical modulation envelope is mapped onto a different optical wavelength. The modulated optical carrier is dispersed in a second spool of SMF28 approximately 5.5km in length. The second dispersion further separates the spectral components of the chirped carrier, causing the electrical modulation envelope to be slowed down in time. The stretch factor is given by $M = 1+D_2/D_1 = 3.75$, where D_1 and D_2 are the total dispersion in the first and second fibres, respectively. It has been shown that the dispersion penalty suffered by the electrical signal is negligible [2].

The results obtained are shown in Fig. 3. The data points are the output of the digitiser and the solid line is an ideal sine wave fit to the data. The output bandwidth has been limited to 4GHz by digital filtering. After stretching, the 5GHz input to the digitiser is slowed down to 1.33GHz. The TSP has increased the effective sampling rate of the electronic digitiser to 30Gsample/s. The measured SNR over the 4GHz bandwidth is 26dB. The SNR was measured by the standard sine-fitting test [3]. It is important to note that this is a real-time test with no averaging, and the measured SNR includes contributions from all noise sources (electronic and photonic) falling within the 4GHz bandwidth.

One of the challenges in such a system is the distortion introduced by the nonuniform spectrum of the chirped pulse. After the pulse is chirped, spectral nonuniformities are mapped into temporal modulation of the carrier, which is subsequently mixed with the input electrical signal in the modulator. This effect produces broadband distortion and is one of the factors currently limiting the bandwidth and the SNR of the TSADC.

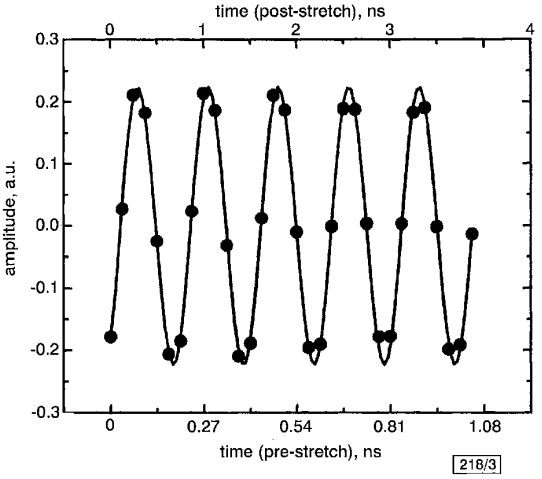

Fig. 3 *Experimental results for time-stretch ADC*

A 5GHz signal is captured at 30Gsample/s with 26dB SNR measured over 4GHz bandwidth

In summary, we have demonstrated a 30Gsample/s TSADC system consisting of a photonic time-stretch preprocessor and an 8Gsample/s electronic digitiser. The system is suitable for capture and analysis of time-limited RF signals.

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Optimal state assignment technique for partial scan designs

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The state assignment of a finite state machine greatly affects the delay, area and testability of sequential circuits. To reduce the length and number of feedback cycles, a new state assignment technique based on m-block partitioning is introduced. Following the completion of the proposed state assignment and logic synthesis stage, partial scan design is performed to choose the minimal number of scan flip-flops. Experimental results show that a drastic improvement in testability can be realised while maintaining a low area and delay overhead.

Introduction: The difficulty of sequential test generation can be alleviated by using full or partial scan designs. Various partial scan design techniques have been proposed [1 – 4]. In [1], a set of flip-flops (FFs) is chosen based on different testability criteria in order to avoid flip-flops that are hard to observe and control. Tar-